Semiconductor Device and Method of Manufacturing the Same

Background of the Invention

1. Field of the Invention~~:~~

The present invention relates to a semiconductor device wherein dummy patterns are formed on a semiconductor substrate together with a wiring pattern, and to a method of manufacturing the semiconductor device.

2. Description of the Related Art~~:~~

In an interlayer film CMP (Chemical mechanical polishing) process, batch polishing has heretofore been performed to reach an intended or target remaining film thickness set value. When, at this time, a polishing pad which is brought into contact with the surface of a wafer is elastically deformed due to pressure from an underlying step at a polishing initial stage, the pressure that is applied from the polishing pad increases when a pattern density is low, whereas the pressure that is applied from the polishing pad is dispersed and becomes low when the pattern density is high, thus causing a difference in the polishing rate between loose and dense wiring pattern loose and dense portions.

Thus, the remaining film thickness differences (hereinafter might be called "global steps") occur among the loose and dense wiring pattern loose and dense portions after polishing. Each of the global steps consists of a difference in film thickness at the loosest

from one another according to a wiring layout. Therefore, when the global step is large in the interlayer film CMP process, the underlying wiring pattern is exposed or disappears at the loose portion of the underlying wiring pattern, and the residual step occurs due to cutting insufficiency at the dense portion ~~thereof~~ of the underlying wiring pattern.

When such exposure, disappearance and residual steps of the underlying wiring pattern occur, no wiring is formed upon forming each wiring in a subsequent process, thus causing degradation in yield and reliability.

Therefore, dummy patterns (pseudo dummy patterns) which are different from an actual wiring pattern are inserted into the entire surface of a chip ~~Chip~~ to set the global steps as low as possible (refer to, for example, a patent document: Japanese Unexamined Patent Publication No. 2003-140319). The global steps vary depending on whether the dummy patterns exist. The insertion of the dummy patterns provides an improvement in the global step.

However, a disadvantage occurs in that when the dummy patterns are inserted, a pattern ratio (pattern proportion) of a mask becomes too large to carry out an end point detector (EPD) upon etching at the formation of a wiring pattern. Therefore, there is a demand for suppressing the insertion of the dummy patterns as low as practicable to thereby reduce the global steps.

While the dummy patterns may preferably be inserted to improve the global steps in this way, a disadvantage occurs in

that when the pattern ratio become excessively large, EPD cannot be detected upon etching of the wiring pattern.

Summary of the Invention

In view of ~~With~~ the foregoing problems ~~in view~~, the present invention therefore provides a semiconductor device which is capable of avoiding an increase in pattern ratio and allowing wiring dummy patterns to improve global steps developed by CMP upon the insertion of the dummy patterns which are different from an actual wiring pattern, and a method of manufacturing the semiconductor device.

The above-described ~~above~~ problems are solved by the following ~~means~~ aspects of the present invention:

A semiconductor device of the present invention comprises a wiring pattern and a plurality of dummy patterns which are different from the wiring pattern, and an insulating film which is formed on the wiring pattern and the dummy patterns by a chemical vapor deposition method. The ~~, wherein the~~ dummy patterns are provided with pattern non-forming regions each having a width which is filled by plus sizing of the insulating film upon formation of the insulating film.

The pattern non-forming regions of the dummy patterns may be formed in stripe form or may be formed in character or graphical form.

In the semiconductor device of the present invention, the pattern non-forming regions of the dummy patterns may preferably

be shaped in character or graphical forms which are different for each ~~every~~ dummy ~~patterns~~ pattern.

In the semiconductor device of the present invention, the dummy patterns may preferably be square. Also, the dummy patterns may preferably be arranged in lattice form.

The present invention also provides ~~On the other hand,~~ a method of manufacturing a semiconductor device, which ~~according to the present invention~~ comprises the following steps of:

forming a wiring pattern;

forming a plurality of dummy patterns which are different from the wiring pattern together with the wiring pattern; and

forming an insulating film on the wiring pattern and the dummy patterns by a chemical vapor deposition method.~~,~~

In ~~wherein in~~ the dummy pattern forming step, the dummy patterns are formed so as to be provided with pattern non-forming regions each having a width which is filled by plus sizing of the insulating film upon formation of the insulating film.

In the dummy pattern forming step, the pattern non-forming regions of the dummy patterns may be formed in stripe form or may be formed in character or graphical form.

In the dummy pattern forming step, the pattern non-forming regions of the dummy patterns may preferably be shaped in character or graphical forms which are different for each ~~every~~ dummy ~~patterns~~ pattern.

In the dummy pattern forming step, the dummy patterns may be shaped in square form. Also, the dummy patterns may be

arranged and formed in lattice form.

In the present invention, dummy patterns formed together with a wiring pattern are respectively provided with pattern non-forming regions each having a predetermined width. The predetermined width of the pattern non-forming region is defined as a width which is filled with an insulating film by plus sizing of the insulating film upon formation of the insulating film. Then, the insulating film is formed on the wiring pattern and the dummy patterns.

Here, the plus sizing of the insulating film is to deposit an insulating film material not only on a pattern upper surface but also on pattern sidewalls upon vapor phase growth of the insulating film and increase the size of each pattern at a predetermined rate. The width of each of the pattern non-forming regions of the dummy patterns is equivalent to the shortest distance between the pattern sidewalls at individual points lying in the pattern non-forming regions.

Therefore, since the pattern non-forming regions are filled with the insulating film material which is deposited on the pattern sidewalls upon vapor phase growth of the insulating film, the coverage of the insulating film remains unchanged at dummy patterns (conventional dummy patterns) which are provided with no pattern non-forming regions and the dummy patterns which are provided with the pattern non-forming regions.

When the formed insulating film is planarized, global steps equivalent to ones which are obtained when the dummy

patters provided with no pattern non-forming regions are provided, can be obtained while reducing a pattern ratio by the provision of the pattern non-forming regions at the dummy patterns.

According to the semiconductor device of the present invention and its manufacturing method, an advantageous effect is achieved ~~brought about~~ in that upon insertion of dummy patterns which are different from an actual wiring pattern, a pattern ratio can be prevented from increasing, and the wiring dummy patterns enable an improvement in the global step of CMP.

Brief Description of the Drawings

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the present invention, it is believed that the present invention, the objects and features of the present invention and further objects, features and advantages thereof will be better understood from the following description when taken in connection with the accompanying drawings in which:

Fig. 1 is a partly plan view (A) and a partly sectional view (B) showing a semiconductor device according to a first embodiment of the present invention;

Fig. 2 is a process view illustrating a method of manufacturing the semiconductor device according to the first embodiment of the present invention;

Fig. 3 is a partly plan view (A) and a partly sectional view (B) showing a semiconductor device according to a second

embodiment of the present invention;

Fig. 4 is a partly plan view (A) and a partly sectional view (B) illustrating a semiconductor device according to a third embodiment of the present invention; and

Fig. 5 is a partly plan view (A) and a partly sectional view (B) depicting a semiconductor device according to a fourth embodiment of the present invention.

Detailed Description of the Invention

The present invention will be described hereinbelow with reference to the accompanying drawings. Incidentally, structural components each substantially having the same function will be explained with the same reference numerals given thereto through all of the drawings.

<First Embodiment ~~embodiment>~~

Fig. 1 is a partially plan view (A) and a partially sectional view (B) showing a semiconductor device according to a first embodiment of the present invention. Fig. 2 is a process view showing a method of manufacturing the semiconductor device according to the first embodiment of the present invention.

In the semiconductor device according to the first ~~present~~ embodiment, as shown in Fig. 1(A), a gate wiring pattern 12 (wiring pattern) is formed on a semiconductor substrate 10, and a plurality of dummy patterns 14 are formed therearound. As shown in Fig. 1(B), a BPSG (Boro Phospho Silicate Glass) oxide film 16 (insulating film) which is planarized by CMP is formed on the

gate wiring pattern 12 and the dummy patterns 14 as an interlayer insulating film. Here, Fig. 1(B) is a sectional view taken along line B - B in Fig. 1(A).

In the dummy patterns 14, stripe-like slits 14b (pattern forming regions) are provided among a plurality of linear patterns 14a.

The width of each of the slits 14b provided at the dummy patterns 14 is set so that ~~as such~~ a width of ~~that~~ the slit 14b is filled by plus sizing of each dummy pattern upon formation of the interlayer insulating film. Described specifically, the width which is filled by plus sizing is 72μm or less, for example.

A method of manufacturing the semiconductor device according to the present embodiment will now ~~next~~ be described.

First, a plurality of dummy patterns 14 are formed on a semiconductor substrate 10 together with a gate wiring pattern 12 by using a gate electrode forming mask (see Fig. 2(A)).

Next, a BPSG oxide film 16 is formed on the gate wiring pattern 12 and the dummy patterns 14 by a chemical vapor deposition method. Since plus sizing of the dummy patterns ~~firstly~~ occurs first at this time, a constituent material used for a BPSG oxide film 16 is deposited from the side surfaces of linear patterns 14a so that slits 14b of the dummy patterns 14 are filled (see Fig. 2(B)). Thereafter, a BPSG oxide film 16 is formed (see Fig. 2(C)).

Then~~Afterwards~~, the surface of the BPSG oxide film 16 is smoothed by CMP (see Fig. 2(D)). The semiconductor device is

fabricated in this way.

In the first ~~present~~ embodiment as described above, the dummy patterns 14 are provided with the slits 14b each having a predetermined width, and the slits 14b are filled by dummy pattern plus sizing upon vapor phase growth of the BPSG oxide film 16. Therefore, the BPSG oxide film 16 is formed at the coverage which is no different from dummy patterns 14 (conventional dummy patterns) with no slits 14b.

Therefore, when the BPSG oxide film 16 is planarized, global steps which are equivalent to ones obtained when the conventional dummy patters are provided, can be obtained while reducing a pattern ratio by the provision of the slits 14b at the dummy patterns 14.

Since the dummy patterns 14 are arranged in lattice form in the first ~~present~~ embodiment, the interval between lattices is varied to make it possible to easily optimize the pattern ratio. It is thus possible to suppress an increase in the global step more effectively.

<Second Embodiment ~~embodiment>~~

Fig. 3 is a partially plan view (A) and a partially sectional view (B) showing a semiconductor device according to a second embodiment of the present invention.

As shown in Fig. 3, the second ~~present~~ embodiment takes a form in which arbitrary graphical ("square" in the second ~~present~~ embodiment) openings 14c (pattern non-forming regions) are respectively provided at the centers of square (square-shaped)

dummy patterns 14. Here, Fig. 3(B) is a sectional view taken along line B - B in Fig. 3(A)~~1(A)~~. Since elements of structure other than the above are similar to those employed in the first embodiment, the description thereof will be omitted.

The first embodiment has explained the form in which the plurality of linear patterns 14a have built up the dummy patterns 14 (the dummy patterns 14 provided with the slits 14b) which are arranged at the predetermined intervals. However~~Since, however~~, since the dummy patterns are constituted of the plurality of linear patterns 14a in this case, the number of graphic forms increases and hence the dummy patterns 14 (linear patterns 14a) are inserted in large numbers. As a result, a problem arises in that since the number of graphic forms increases as compared with the capacity of a design data file (GDS2 data) at the insertion of mere square dummy patterns (dummy patterns 14 with no slits 14b), data capacity is inevitable and its practical handling ~~handing~~ is inconvenient.

Thus, the square dummy patterns 14 which are provided with the arbitrary graphical openings 14c at their centers are formed to thereby suppress an increase in the number of graphical forms in the second ~~present~~ embodiment. The width of the opening 14c is similar to the width of the slit 14b employed in the first embodiment. Also, the form of the opening 14c is not limited to the square but can be configured as any other ~~an~~ arbitrary graphical form.

Therefore, the second ~~present~~ embodiment is capable of

obtaining a global step which is equivalent to one obtained where the conventional dummy patterns are provided, while reducing the pattern ratio by the provision of the opening 14c at each dummy pattern 14, in a manner similar to the first embodiment. Further, the second ~~present~~ embodiment is capable of reducing the design data file capacity (GDS2 data) and improving its practical handling.

~~<~~Third Embodiment ~~embodiment>~~

Fig. 4 is a partially plan view (A) and a partially sectional view (B) showing a semiconductor device according to a third embodiment of the present invention.

The present embodiment takes a form in which arbitrary character-shaped ("A" in the third ~~present~~ embodiment) openings 14c (pattern non-forming regions) are respectively provided at the centers of square dummy patterns 14 as shown in Fig. 4. Here, Fig. 4(B) is a sectional view taken along line B - B in Fig. 4(A)~~1(A)~~. Since elements of structure other than the above are similar to those employed in the second embodiment, the description thereof will be omitted.

In the third ~~present~~ embodiment, the gate wiring pattern 12 and the dummy patterns 14 can be easily identified since the shapes of the openings 14c are represented in arbitrary character form.

~~<~~Fourth Embodiment ~~embodiment>~~

Fig. 5 is a partly sectional view showing a semiconductor device according to a fourth embodiment of the present invention.

The fourth ~~present~~ embodiment takes a form in which square dummy patterns 14 are respectively provided with arbitrary character-shaped or graphical ("numerals" in the fourth ~~present~~ embodiment) openings 14c (pattern non-forming regions) which are different for each of the ~~every~~ dummy patterns 14 as shown in Fig. 5. Since the fourth ~~present~~ embodiment is similar to the third embodiment except for the above, the description of the similar ~~excepted~~ elements of structure will be omitted.

Since the shapes of the openings 14c are set to the character-like or graphical forms which are different for each of the ~~every~~ dummy patterns 14 in the fourth ~~present~~ embodiment, the dummy patterns 14 can be used as addresses. It is thus possible to easily identify a specific pattern lying in the semiconductor device.

Although any of the embodiments has explained the gate electrode pattern as the wiring pattern by way of illustration, the present invention is not limited ~~to it~~ thereto. The present invention can be applied even to a metal wiring pattern which is formed upon wiring multilayering, 3-dimensioning of a semiconductor device or the like. Although the BPSG oxide film has been described as the interlayer insulating film by way of illustration, the present invention is not limited ~~to it~~ thereto. For example, one that causes a similar phenomenon, such as a high density plasma CVD (High Density Plasma-Chemical Vapor Deposition: HDP-CVD) oxide film is also applicable.

While the present invention has been described with

reference to the illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the present invention, will be apparent to those skilled in the art with ~~on~~ reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments which ~~as~~ fall within the true scope of the present invention.

Abstract of the Disclosure

A ~~Disclosed herein are a~~ semiconductor device which is capable of avoiding an increase in pattern ratio and allowing wiring dummy patterns to improve global steps developed by CMP upon insertion of the dummy patterns which are different from an actual wiring pattern. The semiconductor device has a configuration wherein a gate wiring pattern is formed on a semiconductor substrate, a plurality of dummy patterns are provided therearound, and a BPSG oxide film which is flattened by CMP is formed on the gate wiring pattern and the dummy patterns as an interlayer insulating film. In the semiconductor device, the dummy patterns are formed so as to include pattern non-forming regions such as slits.